INTEGRATED DUAL FREQUENCY NOISE ATTENUATOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is directed to a by-pass or attenuator device and more specifically to a miniaturized ceramic device intended to attenuate noise at two discrete frequencies. Without limitation, a particular utility of the device is as a noise attenuator in so-called dual mode cellular phones having both a digital and an analog output. In devices of this sort, where transmission is effected simultaneously on two discrete frequencies, it is desirable to minimize the "noise" generated by each of the two frequencies.

2. Prior Art

Conventional practice in respect of the recently developed dual mode cellular phones is to provide discrete LC networks tailored to attenuate (shunt to ground) the noise generated in the respective digital and analog transmission circuits. With the current trend to miniaturization, the requirement of utilizing discrete components to be attached to the motherboard is undesirable in that the multiple components occupy precious "geography".

Perhaps, more importantly, in the ultra high frequencies involved in cellular technology (900 MHz for analog transmissions and 1.9 GHz for digital transmissions) the inclusion of lead paths to the respective separate components results in a great variation in inductances, since the lead paths themselves function as inductors.

The references noted below were obtained as a result of a prior art search in respect of the instant invention.

U.S. Pat. No. 5,430,601 discloses a MLC which includes a resistance connection.

U.S. Pat. No. 5,170,317 discloses a MLC which includes, in addition to the conventional electrodes, a "correction" electrode which is narrower than the major electrodes to enable the provision of a capacitor having a precise value.

U.S. Pat. No. 4,758,922 discloses a U-shaped "strip line" which functions as a resonance element (capacitor) having ground plane layers and intervening dielectric layers.

U.S. Pat. No. 4,479,100 relates to an impedance matching network which includes a plurality of electrodes of different cross-sectional areas. The electrodes are connectable in parallel with a major electrode to provide a selected desired capacitance.

U.S. Pat. No. 4,074,340 discloses a MLC which includes adjusting electrodes extending to side surfaces of the monolith. Capacitance adjustment is effected by externally connecting or disconnecting the adjusting electrodes with the major electrodes.

U.S. Pat. Nos. 4,048,593 and 2,758,256 disclose the concept of providing a multiplicity of discrete capacitors formed on a single substrate.

SUMMARY OF THE INVENTION

The present invention is directed to a ceramic integrated dual frequency noise attenuator device. More particularly, the invention is directed to an attenuator device adapted to provide a low impedance path to ground at two discrete frequencies.

Still, more particularly, the invention is directed to a dual frequency by-pass device characterized in that the same is extremely simple to manufacture and provides accurate and precisely controlled dual LC circuits.

Still, more particularly, the invention is directed to a single or multilayer by-pass device especially adapted for noise filtration, the device comprising a pair of U-shaped electrodes in a monolithic ceramic dielectric structure. Each of the electrodes includes a base and a pair of leg portions extending from the base. In the monolithic structure each base is disposed at a margin of the monolith, the legs of each U being directed toward the base of the opposite U, the electrodes being disposed on opposite surfaces of the ceramic dielectric.

A characterizing feature of the device is that the overlapping area defined by one pair of legs differs from the overlapping area defined by the second pair of legs, such that two discrete capacitances are formed. The differential overlap may be achieved by one pair of legs being longer than the other pair or by one pair of overlapping legs being wider than the other pair, or by combinations of these factors.

A further characterizing feature of the invention resides in the composite of the branches of the U coupled with the base of the U functioning as an inductor whereby the device, by the provision of the U-shaped electrode combination described, inherently provides a circuit comprised of two capacitors of different values connected in parallel, in series with a pair of inductors defined by the electrodes which also form the capacitance together with the base portions of the U configurations. Where the differential capacitance is provided by the overlapping legs being longer on one side of the U than the legs of the opposite side of the U, there will inherently be provided a proportionately greater inductance due to the longer conductive path of the longer legs.

A further feature of the invention resides in the ability, due to the U-shaped configuration of the electrodes, to increase the inductance by elongating the base of the U, whereby it is feasible to provide an increased inductance without materially increasing the capacitance.

The device of the invention provides a compact and readily manufactured component providing optimal by-pass and noise reduction in a single chip having but two leads (surface-mount or wire) to be connected to the motherboard. By minimizing the external conductive path, a great degree of control of the characteristics of the by-pass device is achieved. This is in contrast to by-pass techniques employing discrete capacitors and inductors which inherently require elongated conductive paths on the PC board and, hence, greater and less controlled inductances.

In accordance with the invention it is an object to provide a readily manufactured integral chip device especially adapted to function as a by-pass or noise reducing device for two discrete frequencies.

A further object of the invention is the provision of a device of the class described wherein the capacitive and inductive values may be precisely determined, the device being compatible with the desired highly efficient use of the geography of the motherboard.

BRIEF DESCRIPTION OF DRAWINGS

FIGS. 1*a* and 1*b* are respectively plan views of the top and bottom electrodes of a device in accordance with the invention.

FIG. 2 is a schematic exploded perspective view of the device of the invention.

FIG. 3 is a diagram of the circuitry defined by the device of the invention.

DETAILED DESCRIPTION OF DRAWINGS

Referring now to the drawings, there is shown in FIG. 2 a schematic exploded perspective of a device in accordance